IN THE CLAIMS

We claim:

1. A liquid crystal display, comprising:

a sapphire substrate having a first crystal lattice structure;

a single crystal silicon structure having a thickness no greater than about 100 nanometers affixed to said sapphire substrate to create a silicon-on-sapphire structure, and a second crystal lattice structure oriented by said first crystal lattice structure;

an array of liquid crystal capacitors formed on said silicon-on-sapphire structure; and

integrated self-aligned circuitry formed from said silicon layer which is operably coupled to modulate said liquid crystal capacitors.

2. The liquid crystal display of claim 1 wherein said sapphire substrate has an r-plane orientation and said single crystal silicon structure has a (100)-orientation.

3. The liquid crystal display of claim 1 wherein each of said liquid crystal capacitors is coupled to a transistor formed on said silicon-on-sapphire substrate.

4. The liquid crystal display of claim 3 wherein each of said liquid crystal capacitors is a nematic liquid crystal capacitor.

5. The liquid crystal display of claim 4 wherein said liquid crystal capacitor provides a reflective pixel element.

6. The liquid crystal display of claim 4 wherein said liquid crystal capacitor provides a pixel element that is transmissible to light.

7. The liquid crystal display of claim 1 wherein each of said liquid crystal capacitors is a ferroelectric liquid crystal capacitor.

8. The liquid crystal display of claim 7 wherein said liquid crystal capacitor provides a reflective pixel element.

9. The liquid crystal display of claim 7 wherein said liquid crystal capacitor provides a pixel element that is transmissible to light.

10. A method for fabricating a monolithically integrated liquid crystal array display and control circuitry on a silicon-on-sapphire structure, comprising the steps of:

a) affixing a sapphire substrate having a first crystal lattice structure to a single crystal silicon structure having a thickness no greater than about 100 nanometers and a second crystal lattice structure oriented by said first crystal lattice structure to create a silicon-on-sapphire structure;

b) ion implanting said single crystal silicon structure with a species selected from the group consisting of silicon ions, tin ions, germanium ions, and carbon ions to create an ion implanted silicon layer;

c) annealing said silicon-on sapphire structure;

d) oxidizing said ion implanted silicon layer to form a silicon dioxide layer from a portion of said silicon layer so that a thinned, ion implanted silicon layer remains;

e) removing said silicon dioxide layer to expose said thinned ion implanted silicon layer;

f) fabricating transistors wherein each of said transistors is formed by patterning said thinned ion implanted silicon layer to create a patterned silicon layer, growing a gate oxide on said patterned silicon layer; forming a polysilicon layer over said silicon-on sapphire structure; doping said polysilicon layer; patterning said polysilicon layer and said gate oxide to form a gate region and to expose selected regions of said thinned, ion-implanted silicon layer; ion implanting said selected regions of said epitaxial silicon layer to create source and drain regions in said thinned, ion-implanted silicon layer that are self-aligned with said gate region;

g) fabricating electrical contacts that are electrically connected to said transistors; and

h) fabricating liquid crystal capacitors on said silicon-on sapphire structure that are electrically connected to said transistors by said electrical contacts.

11. The method of claim 10 wherein said sapphire substrate has an r-plane orientation and said single crystal silicon structure has a (100)-orientation.

12. The method of claim 10 wherein said transistors include nonlinear circuit elements.

13. The method of claim 10 wherein said liquid crystal capacitors include nematic liquid crystal capacitors.

14. The method of claim 10 wherein said liquid crystal capacitors include ferroelectric liquid crystal capacitors.

15. The method of claim 10 further includes fabricating polarizers on said silicon-on-sapphire structure.

16. The method of claim 10 further includes forming a layer of optical filters on said silicon-on sapphire structure.

17. The method of claim 10 includes the steps of:

implanting said silicon ions at a dosage of about 10^{14} cm^{-2}, at an energy level of about 185 keV and, at a temperature of about -20°C;

immersing said silicon-on-sapphire structure in a nitrogen atmosphere having a temperature of about 550°C for approximately 30 minutes;

increasing the temperature of said nitrogen atmosphere in which said silicon-on-sapphire structure is immersed from about 550°C to about 900°C in about one hour;

annealing said silicon-on sapphire structure in said nitrogen atmosphere for about one hour at 900°C; and

oxidizing said silicon layer in an oxygen atmosphere having a temperature of about 1000°C.